IEEE International Symposium on Integrated Circuits and Systems (ISICAS 2024)

Start	End	Duration	Session 1 (Viceroy 1)	Session 2 (Viceroy 2)	Session 3 (Viceroy 3)
Day 1 | 18 October 2024 | Friday					
8:30	9:00	0:30	**Welcome/Registration**		
9:00	9:30	0:30	**Inauguration Ceremony** Shri. Sudhir Marwaha, Group Coordinator / Scientist-G, Ministry of Electronics and Information Technology (MeitY) Government of India Manuel Delgado-Restituto, Past President IEEE Circuits and Systems Society		
9:30	10:00	0:30	**Visionary Keynote Talk : AI-Assisted Design Automation of Analog Circuits: An Overview of The State of the Art and Challenges** **Distinguished Speaker: José M. de la Rosa, Ph.D., Professor, IEEE Fellow**		
10:00	11:00	1:00	**Panel Discussion : SKILLING SEMICONDUCTORS FOR ALL** Sunny Malhotra, Strategy Advisor at Kaynes Semiconductors and RK Electronics,Chairman of IES (NCR Chapter) Shanthi Pavan, IIT Madras, India Francois Rivet, IMS Laboratory Bordeaux, France Nitin Kishore, CEO Truechip Solutions NCR, India		
11:00	11:30	0:30	**Tea / Coffee Break**		
11:30	13:00	1:30	**Technical Papers Session: 1A** **Power Management and Wireless**	**Technical Papers Session: 1B** **Digital Circuits**	**Session: 1C**
11:30	11:50	0:20	**PID_22 : On-chip Configurable RF Energy Harvester for Biomedical Implantable Devices** [Nagaveni S (IIT Dharwad); Praveen Hunasigidad (IIT Dharwad); Deepali Pathak (IIT Hyderabad); Ashudeb Dutta (IIT Hyderabad)]	**PID_43 : An N/PBTI-Isolated BTI Monitor With a Configurable Switching Network and Calibration for Process Variation in Memory Periphery** [Shin-Hyun Jeong (Seoul National University); Yong-Un Jeong (Seoul National University); Suhwan Kim (Seoul National University)]	**IEEE CASS Biltz**
11:50	12:10	0:20	**PID_20 : A High-PSRR NMOS LDO Regulator with Intrinsic Gain-Tracking Ripple Cancellation Technique** [Jung Sik Kim (Hanyang University, South Korea); Seunggyun Ha (Hanyang University, South Korea); Hongyup Jeong (Hanyang University, South Korea); Jeongjin Roh (Hanyang University, South Korea)]	**PID_45 : A 6-Gbps 16-nm FinFET CMOS I/O Buffer With Variation Insensitivity Ensured By Genetic Algorithm** [Chua-Chin Wang (National Sun Yat-sen University (NSYSU), Taiwan); L S S Pavan Kumar Chodisetti (National Sun Yat-sen University (NSYSU), Taiwan); Jhih-Ying Ke (National Sun Yat-sen University (NSYSU), Taiwan); Cheng-Yao Lo (National Sun Yat-sen University (NSYSU), Taiwan); Tzung-Je Lee (National Sun Yat-sen University (NSYSU), Taiwan); Lean Karlo Santos Tolentino (Technological University of the Philippines, Philippines)]	
12:10	12:30	0:20	**PID_23 : A DVS-Enabled Distributed Digital LDO Providing Rapid Uniform Power Grid and Ripple Reduction Achieving 20.1-ps FOM in 28nm CMOS** [Yuli Han (Kyungpook National University); Jaemin Kim (Korea Advanced Institute of Science and Technology (KAIST), Daejeon, South Korea); Gunmo Koo (Kyungpook National University, Daegu, South Korea); Jaejin Kim (Kyungpook National University); Jusung Kim (Hanbat National University, Daejeon, South Korea); Joo-Young Kim (Korea Advanced Institute of Science and Technology (KAIST), Daejeon, South Korea); Kunhee Cho (Kyungpook National University)]	**PID_44 : An M-metric Readout Circuit for MLC Phase Change Memory with a Comparator-Based Push-Pull Bit-Line Driver** [Seo, Min-Jae (University of Seoul)]	
12:30	12:50	0:20	**PID_27 : Enhancing Continuous Beam Angle Resolution for Next Generation Wireless Systems: A Multi-Stage Phase-Shifting Polyphase Filters Approach** [Adam Slater (Washington State University); Hesam Abbasi (Washington State University); Sreeni Poolakkal (Washington State University); Foad Behesti (Washington State University); Subhanshu Gupta (Washington State University)]	**PID_48 : BiNPU: A 33.0 MOP/s/LUT Binary Neural Network Inference Processor Showing 88.26% CIFAR10 Accuracy with 1.9 Mbit On-Chip Parameters in a 28 nm FPGA** [Gil-Ho Kwak (Korea Aerospace University); Tae-Hwan Kim (Korea Aerospace University)]	
12:50	13:00	0:10	**Session 1A wrap up**	**Session 1B wrap up**	
13:00	14:00	1:00	**Lunch Break**		
14:00	15:30	1:30	**Technical Papers Session: 2A** **Power Management and Communcation**	**Technical Papers Session: 2B** **Analog Techniques I**	
14:00	14:20	0:20	**PID_2 : Ultra-Low-Power High PSRR Sub-1V Voltage Reference Circuit in 22nm FDSOI CMOS** [Adilet Dossanov (Technische Universität Braunschweig, Germany); Christian Ziegler (Technische Universität Braunschweig, Germany); Vadim Issakov (Technische Universität Braunschweig, Germany)]	**PID_1 : An Offset-Cancellation Technique Using Charge-Trap Transistors and Asynchronous Programming Scheme** [Ye Lin (Nanjing University); Anying Jiang (Nanjing University); Jingjing Lv (Nanjing University); Yuan Du (Nanjing University); Li Du (Nanjing University)]	
14:20	14:40	0:20	**PID_26 : A Wireless-Powered Battery-Less Electrical Stimulator with Delay-Shift Keying (DSK); Based Downlink Data Communication** [Dao-Han Yao (National Yang Ming Chiao Tung University); Chia-Ching Hung (National Yang Ming Chiao Tung University); Wen-Po Lo (National Yang Ming Chiao Tung University); Po-Hung Chen (National Yang Ming Chiao Tung University)]	**PID_4 : 0.4-V Supply, 12-nW Reverse Bandgap Voltage Reference with Single BJT and Indirect Curvature Compensation** [Chon-Fai Lee (University of Macau); Chi-Wa U (University of Macau); Rui P. Martins (University of Macau and Universidade de Lisboa); Chi-Seng Lam (University of Macau)]	
14:40	15:00	0:20	**PID_28 : A 102-Gb/s/lane 1.4-Vppd Linear Range PAM-8 Receiver Frontend with Multi-Path Continuous-Time Linear Equalization in 28-nm CMOS** [Sangwan Lee (Hanyang University); Hyeongmin Seo (Hanyang University); Seungwoo Son (Hanyang University) Sunoh Yeom (Hanyang University); Jaeduk Han (Hanyang University)]	**PID_25 : A Phase Interpolated Dual-Phase Adaptive On-Time Controlled Buck Converter** [Tsai, Chieh-Ju (National Taiwan University); Chen, Hsiao-Hsuan (National Taiwan University); Chen, Ching-Jan (National Taiwan University)]	
15:00	15:20	0:20	**PID_29 : A 3×12-Gb/s 1.26-pJ/b Single-Ended PAM-3 Transmitter with Crosstalk Cancellation Technique in 28-nm CMOS** [Dongwoo Kang (Yonsei University); Han-Gon Ko (ONE Semiconductor); Kwanseo Park (Yonsei University)]	**PID_49 : Precise Individual Illumination Control of Matrix LED with Bypass Gate Driver and 8-bit PWM** [Jong Hyuk Chae (Sogang University); Jaehun Jeong (Sogang University); Byeongha Park (Sogang University); Seungju Lee (Sogang University); Jongmin Park (Sogang University); Jinwook Burm (Sogang University)]	
15:20	15:30	0:10	**Session 2A wrap up**	**Session 2B wrap up**	
15:30	16:00	0:30	**Tea / Coffee Break**		
16:00	17:30	1:30	**Technical Papers Session: 3A** **Frequency Generation and Wireline**	**Technical Papers Session: 3B** **Analog Techniques II**	
16:00	16:20	0:20	**PID_30 : A 0.09-pJ/b/dB 28-Gb/s Digital CDR with ISI-Resistant Phase Detector** [Suil Kang (Yonsei University); Dongwoo Kang (Yonsei University); Sinho Lee (Yonsei University) Minkyo Shim (Yonsei University); Seungha Roh (Yonsei University); Sunjin Choi (Yonsei University) Kwanseo Park (Yonsei University)]	**PID_6 : A High-Voltage Differential SPDT T/R Switch for Ultrasound Systems** [Yaohua Zhang (University College London); Dai Jiang (University College London); Andreas Demosthenous (University College London)]	
16:20	16:40	0:20	**PID_31 : High-Precision Built-In Phase Noise Measurement Circuit with a Hybrid ΔΣ Time-to-Digital Converter for SoC Clocking Applications** [Jihun Choi (Hanyang University); Sangwook Na (Hanyang University); Hojin Kim (Samsung Electronics); Hyungdong Roh (Samsung Electronics) Youngjae Cho (Samsung Electronics); Michael Choi (Samsung Electronics); Min-Seong Choo (Hanyang University); Jeongjin Roh (Hanyang University)]	**PID_8 : A 10.23-bit ENOB 1 kS/s Differential VCO-based ADC with Resistive Input Stage in Low-Temperature Poly-Silicon TFT Technology** [Yuqing Lou (Shanghai Jiao Tong University, Shanghai, China); Hanbo Zhang (Shanghai Jiao Tong University, Shanghai, China);Jun Li (Shanghai Jiao Tong University, Shanghai, China); Chen Lin (Tsinghua University, Beijing, China);Leilai Shao (Shanghai Jiao Tong University, Shanghai, China); Xiaojun Guo (Shanghai Jiao Tong University, Shanghai, China); Yongfu Li (Shanghai Jiao Tong University, Shanghai, China); Guoxing Wang (Shanghai Jiao Tong University, Shanghai, China); Fakhrul Rokhani Jian Zhao (Universiti Putra Malaysia, Selangor, Malaysia)]	
16:40	17:00	0:20	**PID_32 : A 5.4-7.4GHz Ultra-Low Jitter Injection-Locked Frequency Tripler with 3rd Harmonic Current Boosting Input Buffer** [Sonam Sadhukhan (Texas Instruments, USA); Arpan Thakkar (Texas Instruments, India); Pranav Kumar (Texas Instruments, India); Saurabh Saxena (Indian Institute of Technology, Madras)]	**PID_12 : Artificial Neural Network Based Calibration for a 12b 250MS/s Pipelined-SAR ADC with Ring Amplifier in 40-nm CMOS** [Bin Liu (Xi'an Jiaotong University, China); Nannan Li (Xi'an Jiaotong University, China); Xuhui Chen (Qingdao Hi-image Tech. Co. Ltd., China); Zhichao Dai (Qingdao Hi-image Tech. Co. Ltd., China); Yufeng Ge (Xi'an Jiaotong University, China); Zheng Jiang (Qingdao Hi-image Tech. Co. Ltd., China); Huanhuan Qi (Xi'an Jiaotong University, China); Jie Zhang (Xi'an Jiaotong University, China); Jinfu Wang (Xi'an Aerosemi Technology Company, China); Xiaofei Wang (Xi'an Jiaotong University, China); Zhenhai Chen (Huangshan University, China and China Electronic Technology Group Corporation); Yan Xue (China Electronic Technology Group Corporation, China); Hong Zhang (Xi'an Jiaotong University, China)]	
17:00	17:20	0:20	**PID_33 : A 32-Gb/s Single-Ended PAM-4 Transceiver with Asymmetric Termination and Equalization Techniques for Next-Generation Memory Interfaces** [Hyuntae Kim (Hanyang University, Seoul, South Korea); Yunseong Jo (Hanyang University, Seoul, South Korea); Sanghun Lee (Hanyang University, Seoul, South Korea); Eunsang Lee (Memory Division, Samsung Electronics, Hwaseong, Gyeonggi-do, South Korea); Young Choi (Memory Division, Samsung Electronics, Hwaseong, Gyeonggi-do, South Korea); Jaewoo Park (Memory Division, Samsung Electronics, Hwaseong, Gyeonggi-do, South Korea); Myoungbo Kwak (Memory Division, Samsung Electronics, Hwaseong, Gyeonggi-do, South Korea); Jung-Hwan Choi (Memory Division, Samsung Electronics, Hwaseong, Gyeonggi-do, South Korea); Youngdon Choi (Memory Division, Samsung Electronics, Hwaseong, Gyeonggi-do, South Korea); Jaeduk Han (Hanyang University, Seoul, South Korea)]	**PID_13 : A 512-nW 0.003-mm2 Forward-Forward Black Box Trainer for an Analog Voice Activity Detector in 28-nm CMOS** [Junde Li (University of Macau, China); Guoqiang Xin (University of Macau, China); Wei-Han Yu (University of Macau, China); Ka-Fai Un (University of Macau, China); Rui P. Martins (University of Macau, China and Universidade de Lisboa, Portugal); Pui-In Mak (University of Macau, China)]	
17:20	17:30	0:10	**Session 3A wrap up**	**Session 3B wrap up**	
17:30	18:00	0:30	**Networking Break**		
18:00	19:00	1:00	**Cultural Evening**		

19:00	20:30	1:30	Ethnic Evening Dinner with Dance and Music		

IEEE International Symposium on Integrated Circuits and Systems (ISICAS 2024)					
Start	**End**	**Duration**	**Session 1 (Viceroy 1)**	**Session 2 (Viceroy 2)**	**Session 3 (Viceroy 3)**
Day 2 | 19 October 2024 | Saturday					
8:30	9:00	0:30	Welcome/Registration		
9:00	9:30	0:30	Visionary Keynote Talk : Implantable neural interfaces. Applications and challenges Distinguished Speaker: Manuel Delgado-Restituto, Past President IEEE Circuits and Systems Society		
9:30	10:00	0:30	Visionary Keynote Talk : Future of Automotive mobility Distinguished Speaker: Amardeep Pumhani, Sr. Director, Digital IP and NXP Semiconductors Noida Site Lead		
10:00	11:00	1:00	WiCASS & YP-CASS Panel Discussion : Elevating Women and Young Engineers to Next Level of Professional Growth Preet Yadav, Head India Innovation Ecosystem NXP Semiconductors and Chair IEEE CASS-CS Chapter Delhi Ms. S Usha, Associate Professor, Sri Sairam Engineering College Yann Deval, Professor, Bordeaux Institute of Technology Harini Kandadai, Staff Engineer, Micron India		
11:00	11:30	0:30	Tea / Coffee Break (WiCAS - YPCAS)		
11:30	13:00	1:30	**Technical Papers Session: 4A** **Power Management and Data Converters**	**Technical Papers Session: 4B** **SoC Building Blocks**	**WiCAS-YPCAS Forum talks:**
11:30	11:50	0:20	**PID_3 : Analysis and Design of a Self-bias Cross-coupled CMOS Rectifier to Enhance Input Power Range** [Terence, Teo Boon Chiat (Nanyang Technological University, Singapore); Lim Wu Cong (Nanyang Technological University, Singapore); Rabeek, S. Mohamed (Nanyang Technological University, Singapore); Raja, M. Kumarasamy (Nanyang Technological University, Singapore); Navaneethan, Venkadasamy (Nanyang Technological University, Singapore); Lim, Xian Yang (Nanyang Technological University, Singapore); Siek, Liter (Nanyang Technological University, Singapore)]	**PID_34 : A Loop-Break Decision Feedback Equalizer for DAC/ADC-DSP-based Wireline Transceivers** [Kim, Donggeon (Daegu Gyeongbuk Institute of Science and Technology (DGIST), South Korea); Choi, Yujin (Daegu Gyeongbuk Institute of Science and Technology (DGIST), South Korea); Lee, Jaewon (Daegu Gyeongbuk Institute of Science and Technology (DGIST), South Korea); Jang, Seoyoung (Daegu Gyeongbuk Institute of Science and Technology (DGIST), South Korea); Song, Sungyu (Daegu Gyeongbuk Institute of Science and Technology (DGIST), South Korea); Braendli, Matthias (IBM Research Europe Zurich Laboratory, Switzerland); Morf, Thomas (IBM Research Europe Zurich Laboratory, Switzerland); Kossel, Marcel (IBM Research Europe Zurich Laboratory, Switzerland); Francese, Pier (IBM Research Europe Zurich Laboratory, Switzerland); Kim, Gain (Daegu Gyeongbuk Institute of Science and Technology (DGIST), South Korea)]	
11:50	12:10	0:20	**PID_7 : Up to 45% Faster Supply Boosted Voltage Sense Amplifier (SBVSA); for High-Speed SRAMs** [Rachit Sharma (Indian Institute of Technology Delhi);Anuj Grover (Indraprastha Institute of Information Technology Delhi); Ajay Shroti Indraprastha Institute of Information Technology Delhi); Shouri Chatterjee (Indian Institute of Technology Delhi)]	**PID_36 : A Configurable ML-KEM/Kyber Key-Encapsulation Hardware Accelerator Architecture** [Hyunseon Kim (Inha University, Incheon, South Korea); Haesung Jung (Inha University, Incheon, South Korea); Ardianto Satriawan (Inha University, Incheon, South Korea); Hanho Lee (Inha University, Incheon, South Korea)]	
12:10	12:30	0:20	**PID_9 : A 4.3 GS/s Time-Interleaved ΔΣ DAC with Temperature-Insensitive Bias and Harmonic Cancellation for Qubit Control** [Jaeyun Park (Seoul National University of Science and Technology); Jaewon Nam (Seoul National University of Science and Technology)]	**PID_35 : Mobile-X: Dedicated FPGA Implementation of the MobileNet Accelerator Optimizing Depthwise Separable Convolution** [HyeonSeok Hong (Seoul National University of Science and Technology); DaHun Choi (Seoul National University of Science and Technology); NamJoon Kim (Seoul National University of Science and Technology); Hyun Kim (Seoul National University of Science and Technology)]	
12:30	12:50	0:20	**PID_11 : A 0.6-V 4-MS/s Asynchronous SAR ADC With 2-bit Conversion/cycle Time-Domain Comparator** [Sanghun Lee (Seoul National University of Science and Technology); Won-Young Lee (Seoul National University of Science and Technology)]	**PID_39 : Accelerated Image Processing through IMPLY-Based NoCarry Approximated Adders** [Fabian Seiler (TU Wien); Nima TaheriNejad (Heidelberg University and TU Wien)]	
12:50	13:00	0:10	**Session 4A wrap up**	**Session 4B wrap up**	
13:00	14:00	1:00	Lunch Break (WiCAS - YPCAS/ Mentorship)		
14:00	15:30	1:30	**Technical Papers Session: 5A** **ADCs and Power Management**	**Technical Papers Session: 5B** **Compute-in-Memory and Power Management**	**IEEE CASS Mentoring Program: Special focus to WiCAS - YPCAS**
14:00	14:20	0:20	**PID_10 : Design Methodology for Compact Single-Channel 3-Stage Capacitor-Array-Assisted Charge-Injection DAC-Based SAR ADC** [Chan-Ho Kye (The University of Suwon); Yu-Jin Byeon (Hanyang University); Kyojin Choo (EPFL); Min-Seong Choo (Hanyang University)]	**PID_14 : An 11T1C Bit-Level-Sparsity-Aware Computing-in-Memory Macro with Adaptive Conversion Time and Computation Voltage** [Ye Lin (Nanjing University); Yuandong Li (Nanjing University); Heng Zhang (Nanjing University); He Ma (Nanjing University); Jingjing Lv (Nanjing University); Anying Jiang (Nanjing University); Yuan Du (Nanjing University); Li Du (Nanjing University)]	
14:20	14:40	0:20	**PID_16 : A 22-nA Quiescent Current, 50-mA Output-Capacitor-Less Low-Dropout Regulator With Multiple-Feedback Loop for IoT Devices** [Raghav Bansal (IIT Delhi); Shouri Chatterjee (IIT Delhi)]	**PID_15 : CLUT-CIM: A Capacitance Lookup Table-Based Analog Compute-in-Memory Macro with Signed-Channel Training and Weight Updating for Nonuniform Quantization** **[Fu, Yuzhao (University of Macau, China); Li, Jixuan (University of Macau, China); Yu, Wei-Han (University of Macau, China); Un, Ka-Fai (University of Macau, China); Chan, Chi-hang (University of Macau, China); Zhu, Yan (University of Macau, China); Martins, Rui (University of Macau, China); Mak, Pui-In (University of Macau, China)]**	
14:40	15:00	0:20	**PID_17 : A Ripple-Based Real-Time Built-In-Resistance Compensation for Switching Battery Charger Achieving Fast Charging** [Geuntae Park (Kyungpook National University, Daegu, South Korea); Seongil Yeo (Kyungpook National University, Daegu, South Korea); Chanjung Park (Kyungpook National University, Daegu, South Korea); Kunhee Cho (Kyungpook National University, Daegu, South Korea)]	**PID_19 : A 2.5-A 3-ns-Response-Time Calibration-Free Hybrid LDO Using Scalable Self-Clocked Stochastic Flash-ADC for In-Loop Quantization** [Tianrui Lyu (Sun Yat-sen University); Zixin Wang (Sun Yat-sen University); Jianping Guo (Sun Yat-sen University)]	
15:00	15:20	0:20	**PID_47 : De-correlation and De-bias Post-processing Circuits for True Random Number Generator** [Ruilin Zhang (Kyoto University); Haochen Zhang (Lenovo, China); Xingyu Wang (Waseda University) Ye Ziyang (University of Tokyo); Kunyang Liu (Kyoto University); Shinichi Nishizawa (Waseda University) Kiichi Niitsu (Kyoto University); Hirofumi Shinohara (Kyoto University)]	**PID_21 : An All NMOS KY-Boost Converter with Double Injection Control for Fast Line and Load Transient Response** [Yu-Ting Hung (National Taiwan University); Chieh-Ju Tsai (National Taiwan University); Ching-Jan Chen (National Taiwan University); Chan-Hsuan Hsu (National Taiwan University); Chun-Yu Hsieh (NovaTek Corporation)]	
15:20	15:30	0:10	**Session 5A wrap up**	**Session 5B wrap up**	
15:30	16:00	0:30	Tea / Coffee Break (WiCAS - YPCAS / mentoring program)		
16:00	17:30	1:30	**Technical Papers Session: 6A** **SoC Building Blocks**	**Technical Papers Session: 6B** **Digital Systems and Power Management**	
16:00	16:20	0:20	**PID_24 : Two-phase Hybrid Buck-Boost Converter with Coupled-Inductors under ZVS Operation for USB PD Bidirectional Conversion** [Yi-Ching Chiu (National Yang Ming Chiao Tung University, Hsinchu, Taiwan); Nan-Hsiung Tseng (National Yang Ming Chiao Tung University, Hsinchu, Taiwan); Chih-Cherng Liao (National Yang Ming Chiao Tung University, Hsinchu, Taiwan); Hao-Wen Guan (National Yang Ming Chiao Tung University, Hsinchu, Taiwan); Po-Shiun Chang (National Yang Ming Chiao Tung University, Hsinchu, Taiwan); Ke-Horng Chen (National Yang Ming Chiao Tung University, Hsinchu, Taiwan); Kuo-Lin Zheng (Chip-GaN Power Semiconductor Corporation, Hsinchu, Taiwan); Ying-Hsi Lin (Realtek Semiconductor Corporation, Hsinchu, Taiwan); Shian-Ru Lin (Realtek Semiconductor Corporation, Hsinchu, Taiwan); Tsung-Yen Tsai (Realtek Semiconductor Corporation, Hsinchu, Taiwan)]	**PID_41 : An Efficient FPGA-based Dilated and Transposed Convolutional Neural Network Accelerator** [Wu, Tsung-Hsi (National Taiwan University); Shu, Chang (National Taiwan University); Liu, Tsung-Te (National Taiwan University)]	
16:20	16:40	0:20	**PID_18 : A 2 μA Iq Passive-Ramp-Adaptive-Extended-TON Controlled Buck Converter Leveraging Clamped Adaptive Biased Error Amplifier to Achieve DVS/Load Transient One-Cycle Recovery Time** [Tsai, Chieh-Ju (National Taiwan University); Chen, Hsiao-Hsuan (National Taiwan University); Chen, Ching-Jan (National Taiwan University)]	**PID_37 : RAW Images-based Motion-assisted Object Detection Accelerator Using Deformable Parts Models Features on 1080p Videos** [Zhang, Ling (ShanghaiTech University); Li, Haoyan (ShanghaiTech University); Zhang, Xiangyu (ShanghaiTech University); Lou, Xin (ShanghaiTech University)]	**Industry Fair**
16:40	17:00	0:20	**PID_46 : Area-Delay-Energy-Efficient Approximate Dividers based on Piecewise Linear Fitting of Surface** [Wu, Chaoyuan (Shenzhen University, Shenzhen, China); Shi, Weiwei (Shenzhen University, Shenzhen, China); Yuan, Yida (WingSemi Technology (Shanghai), Shanghai, China); Zou, Zhuoliang (Shenzhen University, Shenzhen, China); Mo, Zhihong (Shenzhen University, Shenzhen, China); He, Jiangwei (Shenzhen University, Shenzhen, China)]	**PID_38 : A Real-Time and High Precision Hardware Implementation of RANSAC Algorithm for Visual SLAM Achieving Mismatched Feature Point Pair Elimination** [Wenzheng He (Xi'an Jiaotong University, China); Zikuo Lu (Xi'an Jiaotong University, China); Xin Liu (Xi'an Jiaotong University, China) Ziwei Xu (Xi'an Jiaotong University, China); Jingshuo Zhang (Xi'an Jiaotong University, China); Chen Yang (Xi'an Jiaotong University, China); Li Geng (Xi'an Jiaotong University, China)]	
17:00	17:20	0:20	**PID_42 : An FPGA-Based Transformer Accelerator with Parallel Unstructured Sparsity Handling for Question-Answering Applications** [Rujian Cao (University of Macau); Zhongyu Zhao (University of Macau); Ka-Fai Un (University of Macau); Wei-Han Yu (University of Macau); Rui P. Martins (University of Macau and Universidade de Lisboa); Pui-In Mak (University of Macau)]	**PID_40 : High Logic Density Cyclic Redundancy Check and Forward Error Correction Logic Sharing Encoding Circuit for JESD204C Controller** [Peng Yin (Henan University); Hongli Chen (Henan University); Yingjun Xia (Henan University); Jinlong Zhang (Henan University); Mingguo Liu (Henan University); Cheng Gu (Henan University); Weizhou Hou (Henan University); Amine Bermak (Hamad Bin Khalifa University); Fang Tang (Chongqing University)]	

17:20	17:30	0:10	Session 6A wrap up	Session 6B wrap up	
17:30	18:00	0:30	Closing Session		