IEEE CASS Satellite Workshop					
Start	**End**	**Duration**	**Session 1 (Viceroy 1)**	**Session 2 (Viceroy 2)**	**Session 3 (Viceroy 3)**
Day 3 | 20 October 2024 | Sunday					
8:30	9:00	0:30	**Welcome/Registration**		
9:00	9:30	0:30	**Inauguration Ceremony**		
9:30	10:00	0:30	**Visionary Keynote Talk**		
10:00	11:00	1:00	**Panel Discussion**		
11:00	11:30	0:30	**Tea / Coffee Break**		
11:30	13:00	1:30	**Session: 1A** **Mixed-Signal Circuits and RF**	**Session: 1B** **System on Chip**	
11:30	11:45	0:15	**W_1: Design techniques for ultra-low-distortion filters and oscillators** [Nagendra Krishnapura (IIT Madras)]	**W_7 : From System to Silicon for More Sustainable Communications** [Francois Rivet (Bordeaux Institute of Technology)]	
11:45	12:00	0:15	**W_2 : Millimeter-wave front ends for 5G phased arrays** [Aniruddhan Sankaran (IIT Madras)]	**W_8 :** [Yann DEVAL (Bordeaux Institute of Technology)]	
12:00	12:15	0:15	**W_3 : Design of Reconfigurable Receiver Architecture for 5G and beyond** [Darshak Bhatt (IIT Roorkee)]	**W_9 : Efficient Circuits and Systems for Next-Generation Cryptography in IoT** [Utsav Banerjee (IISc Bangalore)]	
12:15	12:30	0:15	**W_4 : Next-gen Interconnects for advanced computing and communication: Trends and challenges** [Rohit Sharma (IIT Ropar)]	**W_10 : High Level Synthesis Based Hardware Security and IP Core Protection (IPP)** [Anirban Sengupta (IIT Indore)]	
12:30	12:45	0:15	**W_5 : Design Techniques for Hybrid Data Converters** [Hitesh Shrimali (IIT Mandi)]	**W_11 : EUV Resists Technology Enables Extension of DRAM Logic Nodes for Next-Generation Semiconductor Chip Manufacturing** [Satinder Kumar (IIT Mandi)]	
12:45	13:00	0:15	**W_6 : An LPTV Compact Delay Line for Sub-6GHz Applications** [Imon Mondal (IIT Kanpur)]	**W_12 : Machine Learning Based Memory Management Systems and It's Approaches** [Sreelakshmi Ganti (Geethanjali College of Engineering and Technology, Hyderabad)]	
13:00	14:00	1:00	**Lunch Break**		
14:00	15:30	1:30	**Session: 2A** **Analog and RF Techniques**	**Session: 2B** **Digital Systems**	
14:00	14:15	0:15	**W_13 : Design and analysis of Interface circuits for energy harvesters** [Ankesh Jain (IIT Delhi)]	**W_19 : Hardware accelerator designs for PQC algorithms** [Makoto Ikeda (University of Tokyo)]	
14:15	14:30	0:15	**W_18 : Process Scalable Digitally Intensive Architectures for Low-Power Sub-Sampling Mixer-First RF front-ends** [Vijayasankara Rao (IIT Bhubaneswar)]	**W_26 : Crossbar based Mixed-Signal Neural Architectures under Variability and Parasitics** [Alex James (Digital University Kerala)]	
14:30	14:45	0:15	**W_15 : Radio Frequency Power Amplifier Design in RFIC/MMIC Technology** [Karun Rawat (IIT Roorkee)]	**W_21 : Multiply Accumulate Engine - Manual Transmission** [Janakiraman Viraraghavan (IIT Madras)]	
14:45	15:00	0:15	**W_16 : Closed-loop Neuromodulation SoCs** [Laxmeesha Somappa (IIT Bombay)]	**W_22 : Chiplets: Revolutionizing Semiconductor Design for High-Performance Computing** [Boon Chong Ang (University of Putra Malaysia , Intel)]	
15:00	15:15	0:15	**W_17 : Energy Efficient Current-Mode Full-Duplex Transceiver for Serial Links** [Nijm Wary (IIT Bhubaneswar)]	**W_23 : On-chip ECG Monitor for Early Detection of Cardio-vascular Diseases** [Bishnu Prasad Das (IIT Roorkee)]	
15:15	15:30	0:15	**W_14 : Floating inverter amplifier: An opamp for switched-capacitor circuits** **[Ashwin Kumar (IIT Kanpur)]**	**W_24 : Variability Aware Models for Metastability Window of CMOS Flip-Flops** [Anand Bulusu (IIT Roorkee)]	
15:30	16:00	0:30	**Tea / Coffee Break**		
16:00	17:30	1:30	**Session: 3A**	**Session: 3B** **Digital**	**Session: 3C** **SRF**
16:00	16:15	0:15		**W_25 :** **[Sudeb Dasgupta (IIT Roorkee)]**	**W_30 : Research and Technology Development in RF Power Amplifiers: RFICs to Modules** [Ganesh Bargaje (IIT Roorkee)]
16:15	16:30	0:15		**W_20 :** VLSI implementation of Threshold Logic Gate [Mili Sarkar (Institute of Engineering and Management, Kolkata.)]	**W_31 : PVT-Insensitive Time Domain-Based In-Memory Computation with Improved Linearity for Machine Learning Applications** [Amandeep Singh (IIT Roorkee)]
16:30	16:45	0:15		**W_27 : Efficient RISC V Compute Platforms for Enabling the AI Revolution** [Sujay Deb (IIT Delhi)]	**W_32 : Implementing a CMOS Potentiostat for Electrochemical Biosensing** [Vishwajeet Prashant Jadhav (IIT Roorkee)]
16:45	17:00	0:15		**W_28 : Reconfigurable RF Receivers for Positioning with Global Navigation Satellite Systems** [Vijay kanchetla (IIT Bombay)]	**TBD**
17:00	17:15	0:15		**Standards** [Srikanth Chandrasekaran (IEEE Standards Association)]	**TBD**
17:15	17:30	0:15			**TBD**
17:30	18:00	0:30	**Closing Session**		